What is claimed is:

1. A semiconductor device, comprising:

a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and

a gate capacitively-coupled to the body and adapted for using a control signal, when the body is reversed biased, to modulate the length of the intermediate region by changing a concentration of carriers in the intermediate region.

2. The semiconductor device of claim 1, wherein the gate is further adapted to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state.

3. The semiconductor device of claim 1, further including means for modulating an electric field within the body to cause the device to transition between a current-conducting state in which the device is in avalanche breakdown condition and a current-blocking state.

4. The semiconductor device of claim 1, wherein a relatively high bias voltage at the gate maintains the device in a current-conducting state in which the device is in an avalanche breakdown condition, and wherein a relatively low bias voltage at the gate maintains the device in a current-blocking state.

5. The semiconductor device of claim 4, wherein the relatively high bias voltage shortens the effective length of the intermediate region.

6. The semiconductor device of claim 1, wherein a relatively low bias voltage at the gate maintains the device in a current-conducting state in which the device is in an avalanche breakdown condition, and a relatively-high bias voltage at the gate maintains the device in a current-blocking state.

7. The semiconductor device of claim 6, wherein the relatively low bias voltage shortens the effective length of the intermediate region.

8. The semiconductor device of claim 1, wherein the gate is located at least preponderantly over the second region.

9. The semiconductor device of claim 1, wherein the gate is located at least preponderantly over the intermediate region.

10. The semiconductor device of claim 1, wherein the gate is located to provide a surface channel nearer the second junction than the first junction.

11. The semiconductor device of claim 1, wherein when the body is reversed-biased, the first region is maintained at a relatively lower voltage level than the second region, the difference in potential of the first and second regions being sufficient to cause a breakdown condition in the intermediate region in response to the control signal modulating the length of the intermediate region and thereby reducing the distance across the intermediate region over which the potential drops.

12. The semiconductor device of claim 1, wherein the intermediate region has a polarity that is neutral relative to the polarity of the first and second regions.

13. The semiconductor device of claim 12, wherein the intermediate region is lightly doped to achieve the polarization of one of the first and second regions, the intermediate region having a substantially lower dopant concentration level, relative to said one of the first and second regions.

14. The semiconductor device of claim 12, wherein the intermediate region is substantially intrinsic.

15. The semiconductor device of claim 1, wherein the gate is further adapted to cause the device to transition between a current-conducting state in which the device is

in an avalanche breakdown condition and a current-blocking state in which substantially no leakage current passes between the first and second regions.

16. The semiconductor device of claim 1, further comprising a controller coupled to the gate and adapted for applying the control signal to change the concentration of carriers in the intermediate region.

17. The semiconductor device of claim 1, wherein the gate is further adapted to increase an electric field in the intermediate region and for causing an avalanche breakdown condition.

18. A semiconductor device comprising:

a multi-region body including a P-type region, an N-type region and an intermediate region having a first junction with the P-type region and a second junction with the N-type region, the body adapted to be reverse biased across the P-type and N-type regions;

a gate coupled via an intervening gate dielectric material to the intermediate region, and offset to present an electric field substantially at only one of the two junctions; and

the gate, the P-type region and the N-type region being adapted and controllable to switch the device between at least two stable conductance states in response to a voltage-bias control signal applied to the gate.

19. The semiconductor device of claim 18, wherein the device is switched between a high-resistance conductance state and a low-resistance conductance state as a function of an avalanche breakdown condition at a field-induced junction in the intermediate region.

20. The semiconductor device of claim 18, wherein the intermediate region has a length that separates the first and second junctions sufficiently to permit the avalanche breakdown condition before another breakdown condition when the body is reverse biased.

21. A memory circuit comprising:

a data storage node;

a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and

a gate coupled to the body via an intervening dielectric material and offset for using a control signal, when the body is reversed biased, to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body.

22. The memory circuit of claim 21, wherein the body and the gate are adapted to access data stored at the data storage node as a function of the avalanche breakdown condition.

23. The memory circuit of claim 21, wherein the body and the gate are adapted to read data from the data storage node as a function of the avalanche breakdown condition.

24. The memory circuit of claim 21, wherein the body and the gate are adapted to write data to the data storage node as a function of the avalanche breakdown condition.

25. The memory circuit of claim 21, wherein a charge at the data storage node is maintained by controlling the body in a reverse biased condition.

26. The memory circuit of claim 21, wherein the body and the storage node are adapted to drain a charge at the storage node in response to the body being placed in a forward biased condition.

27. A memory circuit comprising:

a data storage node;

a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and

a gate coupled to the body via an intervening dielectric material and offset for using a control signal, when the body is reversed biased, to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes through the body as a function of a charge at the data storage node.

28. The memory circuit of claim 27, wherein the data storage node is coupled to the gate, the gate responding to a charge at the data storage node by presenting the electric field.

29. The memory circuit of claim 27, further comprising a sense device coupled to the body and adapted to detect data stored at the data storage node in response to current passing through the body.

30. A memory circuit comprising:

a data storage node;

first and second multi-region bodies, each body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction;

a first gate coupled to the first body via an intervening dielectric material and offset for using a control signal, when the first body is reversed biased, to present an electric field substantially at only one of the first and second junctions of the first body, the first body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the data storage node and the first body; and

a second gate coupled to the data storage node and to the second body via an intervening dielectric material and adapted for using a charge at the data storage node, when the second body is reversed biased, to modulate an electric field in the intermediate region of the second body, the second body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the second body is in an avalanche breakdown condition and current passes through the second body.

31. The memory circuit of claim 30, further comprising a sense device coupled to the second body and adapted to detect data as a function of sensed current passing through the second body, and wherein the second gate is further adapted to influence an electric field substantially at only one of the first and second junctions.

32. A semiconductor device, comprising:

a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and

first and second gates coupled to the body via intervening dielectric material and adapted for using control signals, when the body is reversed biased, to present an electric field at one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition.

33. The semiconductor device of claim 32, wherein the first gate is adapted to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, the body being held in a steady state without the avalanche breakdown condition occurring absent a similarly-biased control signal capacitively coupled to the body from the second gate.

34. The semiconductor device of claim 32, wherein the first gate is adapted to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, the body switching

to the current-conducting state in response to a second voltage-bias control signal being capacitively coupled to the body, the first and second voltage-bias control signals being of similar bias.

35. The semiconductor device of claim 32, wherein the second gate is responsive to temperature and adapted to apply a control signal to the body that counters temperature-related effects that alter the creation of the avalanche breakdown condition in response to a control signal being applied by the first gate.

36. The semiconductor device of claim 35, wherein the second gate is adapted to apply the control signal to maintain a threshold voltage level in the intermediate region, the threshold voltage being a minimum amount of additional voltage applied to the intermediate region for causing the avalanche breakdown condition.

37. An inverter circuit comprising:

first and second multi-region bodies, each body having a highly-doped P-type region that extends to a first junction, a highly-doped N-type region that extends to a second junction, and an intermediate region having a neutral polarity relative to the P-type and N-type regions and having a length extending from the first junction to the second junction, the N-type region of the first body and the P-type region of the second body being coupled to a common output node;

first and second gates respectively capacitively coupled to the first and second bodies and each adapted, when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions; and

an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node.

38. A semiconductor device comprising:

a relatively thin intermediate region defined by sides including an upper portion and a sidewall portion;

a first region dominated by a first polarization that extends to a first junction with the intermediate region;

a second region dominated by a second polarization that extends to a second junction with the intermediate region; and

a gate extending around and capacitively coupled to at least two sides of the intermediate region for coupling a voltage to the intermediate region, when the first and second regions are reversed biased, to present an electric field substantially at only one of the first and second junctions, the device responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes through the intermediate region.

39. A semiconductor device, comprising:

a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and

means for presenting, when the body is reversed biased, an electric field at the first junction, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body.

40. A method for operating a semiconductor device having a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction and an intermediate region having a length extending from the first junction to the second junction, the method comprising:

capacitively coupling an electric field to the body at the first junction, when the body is reversed biased, and causing the body to switch from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body.

41. The method of claim 40, further including modulating an electric field within the body to cause the body to transition between a current-conducting state in which the body is in avalanche breakdown condition and a current-blocking state in which substantially no current flows between the first and second regions.

42. A method for manufacturing a semiconductor device including a multi-region body, the method comprising:

doping a first region of the body to a first polarization that extends to a first junction;

doping a second region of the body to an opposite polarization that extends to a second junction, the first and second junctions defining a length of an intermediate region extending between the first and second regions; and

forming a gate capacitively-coupled to the body and arranged with the body for using a control signal to present, when the body is reversed biased, an electric field at the first junction that causes the body to switch from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body.

43. A semiconductor device, comprising:

a multi-region body having an upper surface and including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having an upper portion over a lower portion and a length extending from the first junction to the second junction;

a gate capacitively-coupled to the body and adapted for using a control signal, when the body is reversed biased, to modulate the length of the intermediate region by changing a concentration of carriers in the intermediate region and thereby causing the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state; and

the avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state.